

**REMARKS**

Reconsideration and further examination of the application, as amended, are respectfully requested. All objections and rejections are respectfully traversed.

In the Office Action, originally filed claims 1-4 were found to be allowable. Applicants have amended claims 1 and 4 to correct several minor, typographical errors.

The Office Action, citing to 37 C.F.R. §1.105, also requests that the Applicants provide a discussion of several references identified in the Office Action. Applicants note that §1.105 does not include a provision for requesting such information from the Applicants. Nonetheless, in response to the request, Applicants state as follows.

Pat. No. 6,125,429 relates to a computing system having multiple CPUs and memory resources connected by a cross-bar switch. The interleaving bits and row address of the main memory address for victim data and fill data, moreover, are common to one another.

Pat. No. 6,209,065 relates to a mechanism for reducing latency of inter-reference ordering between sets of memory reference operations among a plurality of symmetric multiprocessor (SMP) nodes interconnected by a hierarchical switch.

Published Pat. Appl. No. 2002/0146022 relates to a credit-based, flow control technique that conserves resources of a switch fabric within a multiprocessor computer system.

Published Pat. Appl. No. 2001/0037435 relates to physical-to-logical address translation mapping and source routing for supporting flexible configuration and partitioning in a modular, shared memory multiprocessor system having a plurality of multiprocessor building blocks interconnected by a switch fabric.

Published Pat. Appl. No. 2003/0076831 relates to a technique for combining ordered components and unordered data components into common packets transmitted over an ordered channel of a multiprocessor computer system having a plurality of nodes interconnected by a hierarchical switch. If the combined packet is stalled, it may be decomposed into ordered and unordered components.

Counsel for the Applicants is not aware of any particular keywords, citations to electronically searchable databases or other indexed collections as mentioned on page 3 of the Office Action.

IDS

Applicants submit an Information Disclosure Statement along with this Response.

New Claims

Applicants have added new claims 5-8. No new matter is being introduced. Support for new claim 5 may be found in the Specification as originally filed at claim 3, among other places. Support for new claim 6 may be found in the Specification as originally filed at p. 8, among other places. Support for new claim 7 may be found in the

PATENTS  
15311-2321  
200308272-1

Specification as originally filed at p. 6, among other places. Support for new claim 8 may be found in the Specification as originally filed at pp. 2-5, among other places.

Applicants submit that the application, as amended, is in condition for allowance and early favorable action is requested.

Authorization to Debit Deposit Account

It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's deposit account no. 08-2025.

Respectfully submitted,



\_\_\_\_\_  
Michael R. Reinemann  
Reg. No. 38,280  
(617) 951-2500

Send all correspondence to:

IP Administration Legal Department,  
M/S 35  
Hewlett-Packard Co.  
P.O. Box 272400  
Fort Collins, CO 80527-2400